In the Claims:

Please cancel claim 19.

Please amend the following claims:

1. (Twice Amended) A method of forming an emitter in a vertical bipolar transistor comprising:

providing a substrate having a collector layer and a base layer over said collector layer, said collector layer and said base layer are formed by implantation through a single mask formed on the substrate;

forming a patterned mask over said base layer; and

filling openings in said mask with emitter material in a damascene process, said emitter material contacting the substrate.

11. (Twice Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector, said collector layer and said base layer are formed by implantation through a single mask formed on the SOI substrate;

forming a gate oxide layer over only said CMOS region of said SOI substrate;

forming a polysilicon layer over a CMOS region of said SOI substrate;

patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region

depositing an emitter material in said openings in a damascene process to form emitters;

removing said mask;

patterning said polysilicon layer to form gate conductors; and

forming sidewall spacers adjacent said emitters and said gate conductors.

Cnt B2 E1

12. (Twice Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector, said collector layer and said base layer are formed by implantation through a single mask formed on the SOI substrate;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

B3 E1

14. (Twice Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector, said collector layer and said base layer are formed by implantation through a single mask formed on the SOI substrate;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors. wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

18. (Once Amended) A method of forming a bipolar device on a SOI substrate having a semiconductor layer overlying a buried insulator layer to form an interface where a surface of the semiconductor layer is adjacent to a surface of the buried insulator layer, comprising the steps of:

forming in said semiconductor layer a buried collector region centered at approximately said interface; and

forming in said semiconductor layer a base region vertically stacked on said buried collector region;

wherein said buried collector region and said base region are formed by implantation through a single mask formed on the SOI substrate.